Analog Zero IF FM Decoder and Embodiments Thereof, Such as the Family Radio Service

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Cross-Reference to Other Applications

This application claims the benefit of U.S. Provisional Application No. 60/116,848, filed January 22, 1999, incorporated herein by reference in its entirety.

The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

"Method and System for Down-Converting Electromagnetic Signals," Serial No. 09/176,022, filed on October 21, 1998.

"Method and System for Frequency Up-Conversion," Serial No. 09/176,154, filed on October 21, 1998.

"Method and System for Ensuring Reception of a Communications Signal," Serial No. 09/176,415, filed on October 21, 1998.

"Integrated Frequency Translation and Selectivity," Serial No. 09/175,966, filed on October 21, 1998.

"Image-Reject Down-Converter and Embodiments Thereof, Such as hte Family Radio Service," Serial No. *to be assigned*, Attorney Docket No. 1744.0240001, filed January 3, 2000.

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"Communication System With Multi-Mode and Multi-Band Functionality and Embodiments Thereof, Such as the Family Radio Service ," Serial No. *to be assigned*, Attorney Docket No. 1744.0260001, filed January 3, 2000.

"Multi-Mode, Multi-Band Communication System," Serial No. *to be assigned*, Attorney Docket No. 1744.0330001, filed January 3, 2000.

Background of the Invention

Field of the Invention

The present invention is generally directed toward receiver-transmitter systems referred to as Family Radio Service (FRS) units, although the invention is not limited to this embodiment. The Family Radio Service (FRS) is one of the Citizens Band Radio Services. It is intended for the use of family, friends, and associates to communicate among themselves within a neighborhood or while on group outings. There are fourteen discreet FRS channels available for use on a "take turns" basis. The FRS unit channel frequencies are:

Channel No.	(MHz)
1	462.5625
2	462.5875
3	462.6125
4	462.6375
5	462.6625
6	462.6875
7	462.7125
8	467.5625
9	467.5875
10	467.6125

11	467.6375
12	467.6625
13	467.6875
14	467.7125

Other selected technical specifications are:

(a) Frequency modulation (although phase modulation is allowed);

(b) Frequency tolerance of each FRS unit must be maintained within 0.00025%;

(c) The authorized bandwidth for an FRS unit is 12.5 KHz; and

(d) Effective radiated power (ERP) shall not, under any condition of modulation, exceed 0.500 W.

The operating rules for the FRS are found at 47 C.F.R. 95.191 - 95.194. For additional technical information, see 47 C.F.R. 95.601 - 95.669.

Related Art

A variety of FRS systems are available. Presently available FRS systems do not directly down-convert FM signals to demodulated baseband information signals.

What is needed is a method and system for directly down-converting FM signals to demodulated baseband information signals.

Summary of the Invention

The present invention is directed to a communications system comprising a method and system for directly down-converting FM signals to demodulated baseband information signals. The invention has a number of aspects, including a ultra-low power down-converter and a high-efficiency transmitter and can be used to directly down-convert analog FM signals and digital FM signals to demodulated baseband information signals. In an embodiment, the present invention is used in a family radio service unit. It is to be understood, however, that the invention is not limited to this particular embodiment. Other implementations in communications-related environments are within the scope and spirit of the invention.

In an embodiment, the invention includes aliasing an FM signal at an aliasing rate substantially equal to the frequency of the FM signal or substantially equal to a sub-harmonic thereof; adjusting the aliasing rate in accordance with frequency changes on the FM signal to maintain the aliasing rate substantially equal to the frequency of the FM signal; and outputting a demodulated baseband information signal.

The invention includes an optional step of compensating for phase delays and/or other characteristics of the loop in order to maintain bandwidth and stability for the loop.

In an embodiment, the invention is implemented as a zero IF FM decoder that down-converts an FM signal as an I and Q pair, sums the I and Q pair, and generates a correction signal from the sum. The correction signal is used to adjust the aliasing rate to continually alias the FM signal at a sub-harmonic of the FM signal - even as the FM signal changes frequency.

In an embodiment, the invention is implemented as an ultra-low power down-converter. In an embodiment, the invention is implemented as a transceiver, which can be an FRS transceiver.

Advantages of the invention include, but are not limited to, power reduction, parts reduction, price reduction, size reduction, performance increase, efficiency, and integration possibilities.

Brief Description of the Figures

FIG. 1 is a high level block diagram of an ultra-low power down-converter in accordance with the present invention.

FIG. 2 is a schematic diagram of an exemplary implementation of the ultra-low power down-converter illustrated in FIG. 1.

FIG. 3 is a detailed block diagram of an aliasing module (i.e., universal frequency translator), in accordance with the present invention.

FIG. 4 illustrates a process for directly down-converting an FM signal to a demodulated baseband information signal.

FIG. 5 is a block diagram of an exemplary zero IF FM decoder for implementing the process of FIG. 4.

FIG. 6A is a timing diagram of an exemplary FM signal.

FIG. 6B is a timing diagram of an exemplary first aliasing signal, in accordance with the present invention.

FIG. 6C is a timing diagram of an exemplary second aliasing signal, in accordance with the present invention.

FIG. 6D is a timing diagram of exemplary down-converted signals and a summation signal, in accordance with the present invention.

FIG. 6E illustrates an exemplary control signal for controlling an aliasing rate for directly down-converting an FM signal to a demodulated baseband information signal, in accordance with the present invention.

FIG. 7 is a schematic diagram of an exemplary implementation of a summing module, an integration module and an optional loop compensation module, in accordance with the present invention.

FIG. 8 is a block diagram of a system for transmitting a voice signal, in accordance with an aspect of the present invention.

FIG. 9 is block diagram of a Universal Frequency Translator (UFT) in accordance with an aspect of the present invention.

FIG. 10 is a schematic diagram of an exemplary implementation of the system for transmitting a voice signal illustrated in FIG. 8.

FIG. 11 illustrates a field effect transistor (FET) that can be used by the present invention.

Detailed Description of the Preferred Embodiments

Family Radio with Zero IF FM Decoder

U.S. Patent Application 09/176,022, titled,"Method and System for Down-Converting Electromagnetic Signals," (hereinafter referred to as the `022 application) incorporated herein by reference in its entirety, discloses methods and systems for directly down-converting EM signals.

The `022 application discloses, among other things, how modulated EM signals can be directly down-converted to demodulated baseband information signals (also referred to interchangeably herein as direct to data or D2D

embodiments). For example, amplitude modulated (AM) signals and phase modulated (PM) signals can be directly down-converted to demodulated baseband information signals by aliasing the AM and PM signals at sub-harmonics of the AM and PM signals.

Frequency modulated (FM) signals, however, pose special challenges. For example, the `022 application discloses how frequency shift keying (FSK) signals, when aliased at fixed sub-harmonic, are down-converted to amplitude shift keying signals or to phase shift keying (PSK) signals. FM signals, unlike AM and PM signals, are not necessarily directly down-converted to demodulated baseband information signals by aliasing at a fixed sub-harmonic.

The present invention is a method and system for directly down-converting FM signals to demodulated baseband information signals.

FIG. 4 is a flowchart 402 that illustrates a method for directly down-converting FM signals to demodulated baseband information signals. FIG. 5 illustrates an exemplary embodiment of a zero IF FM decoder 502, which can be used to implement the process illustrated in the flowchart 402. The process illustrated in the flowchart 402 is not, however, limited to the zero IF FM decoder 502. Upon reading this disclosure, one skilled in the relevant art(s) will recognize that the process illustrated in the flowchart 402 can be practiced by other systems as well.

The zero IF FM decoder 502 includes a first aliasing module 510 and a second aliasing module 512. Preferably, the first and second aliasing modules 510 and 512 are implemented as disclosed in the `022 application and may be optimized as illustrated in FIGS. 1-3 of the present application and as described above. Other components of the zero IF FM decoder 502 are described below with the description of the process flowchart 402.

The process begins at step 410, which includes aliasing an FM signal at an aliasing rate substantially equal to the frequency of the FM signal or substantially equal to a sub harmonic thereof.

In FIG. 5, step 410 is performed by the first and second aliasing module 510 and 512. The first aliasing module 510 receives an FM signal 514 and a first a LO signal 516. The first LO signal 516 is substantially equal to the frequency of the FM signal 514 or a sub-harmonic thereof. Details of maintaining the LO signal 516 at the frequency of the FM signal 514, or a sub-harmonic thereof, is described in connection with step 412 below. The first aliasing module 510 uses the first LO signal 516 to down-convert the FM signal 514 to a first down-converted signal 518, as disclosed in the `022 application.

The second aliasing module 512 also receives the FM signal 514 and a second LO signal 520. The first LO signal 516 and the second LO signal 520 are substantially similar except that one is shifted in phase relative to the other. This is performed by, for example, a phase shifter 524. A variety of implementations of the phase shifter 524 suitable for the present invention are available as will be apparent to persons skilled in the relevant art, based on the teachings herein.

In an exemplary embodiment, the first and second LO signals 516 and 520 are separated by ¼ period of the FM signal 514, or any multiple of a period of the FM signal 514 plus ¼ period. Other phase differences are contemplated and are within the scope of the present invention. The second aliasing module 512 uses the second LO signal 520 to down-convert the FM signal 514 to a second down-converted signal 522, as disclosed in the `022 application.

Step 412 includes adjusting the aliasing rate in accordance with frequency changes on the FM signal to maintain the aliasing rate substantially equal to the frequency of the FM signal.

The `022 application teaches that, so long as an aliasing rate remains substantially equal to the frequency of an FM signal, the resultant down-converted

signal is substantially a constant level. In the case of the zero IF FM decoder 502, therefore, the first and second down-converted signals 518 and 522 should generally be constant signals.

In order to maintain this condition, the zero IF FM decoder 502 maintains the phase of the aliasing signal 538 so that the phase of one of the aliasing signals 516 or 520 slightly leads the FM signal 514 while phase of the other aliasing signal slightly lags the FM signal 514.

As a result, one of the down-converted signals 518 or 522 is a constant level above DC while the other down-converted signal is a constant level below DC. The sum of the down-converted signals 518 and 522 is thus substantially zero. Summation of the down-converted signals 518 and 522 is performed by a summing module 526, which outputs a summation signal 536.

When summation signal 536 tends away from zero, it indicates that the frequency of the FM signal 514 is changing. The summation signal 536 is integrated by an integrator module 528, which outputs a control signal 532. The control signal 532 controls a voltage controlled oscillator (VCO) 534, which outputs the aliasing signal 538. The integrator maintains the control signal at a level necessary to insure that the FM signal 514 is aliased at a sub harmonic of the FM signal - even as the FM signal 514 changes frequency.

FIG. 7 illustrates, among other things, exemplary implementation details of the summing module 526 and the integrator module 528. A variety of other implementations of the summing module 526 and the integrator module 528, suitable for the present invention, are available, as will be apparent to persons skilled in the relevant art, based on the teachings herein. A variety of implementations of the VCO 534 suitable for the present invention are also available as will be apparent to persons skilled in the relevant art, based on the teachings herein.

FIGS. 6A-6D illustrate exemplary timing diagrams for the above description. FIG. 6A illustrates an exemplary FM signal 514. FIG. 6B illustrates a first aliasing signal 612, which is generated within the first aliasing module 510 from the first LO signal 516. FIG. 6C illustrates a second aliasing signal 614, which is generated within the second aliasing module 512 from the second LO signal 520. The first and second aliasing signals 612 and 614 are separated by approximately ¼ period of the FM signal 514.

In operation, the first LO signal 612 aliases the FM signal 514 at approximately the same positive position on successive periods. The result is illustrated in FIG. 6D as down-converted signal 518. Similarly, the second LO signal 614 aliases the FM signal 514 at approximately the same negative position on successive periods. The result is illustrated in FIG. 6D as down-converted signal 522. FIG. 6D illustrates the sum of the down-converted signals 518 and 522 as summation signal 536.

When the frequency of the FM signal 514 changes, summation signal 536 tends away from zero. When this happens, the output of the integrator module 528 - i.e., control signal 532 - changes accordingly so that the VCO 534 changes the aliasing rate of the aliasing signal 538 so that the sum of the down-converted signals 518 and 520, summation signal 536, is maintained at zero. Thus, the control signal 532 changes in proportion to frequency changes on the FM signal 514. The changes on the FM signal 514 form a demodulated baseband information signal, which represents the information that had been frequency modulated on the FM signal 514.

In other words, as the frequency of the FM signal 514 changes, the integrator module 528 changes the control signal 532 to track and follow the deviation. This will reproduce – within the bandwidth of the loop – any arbitrary wave form, including analog and digital.

Another way of explaining it is to say that the invention tracks frequency changes on the FM signal by aliasing the FM signal at a sub-harmonic of the FM signal, adjusting the aliasing rate as necessary to maintain the aliasing rate at the sub-harmonic - even as the FM signal changes frequency.

In this way, the aliasing rate changes in proportion to frequency changes on the FM signal. Thus, changes to the aliasing rate are directly indicative of the information modulated on the FM signal. In the exemplary embodiment of FIG. 5, changes to the aliasing rate are indicated by the control voltage 532, which controls the VCO 534, which determines the aliasing rate.

FIG. 6E illustrates an exemplary control signal 532 for controlling the aliasing rate for directly down-converting the exemplary FM signal 514 illustrated in FIG. 6A to a demodulated baseband information signal. In this example, the control signal 532 has a first amplitude during time T1, when the FM signal 514 is at a first frequency. The control signal 532 has a second amplitude during time T2, when the FM signal 514 is at a second frequency. The control signal 532 reverts to the first amplitude during time T3, when the FM signal 514 returns to the first frequency. One skilled in the relevant art(s) will recognize, based on the disclosure herein, that the timing diagrams of FIGS. 6A-6E are exemplary illustrations of the invention. Other timing diagrams will apply for different situations, all of which are within the scope of the present invention.

Step 414 includes outputting a demodulated baseband information signal. In FIG. 5, this is performed by outputting the control signal 532 as a demodulated baseband information signal

An optional step 416 includes compensating for phase delays and/or other characteristics of the loop in order to maintain bandwidth and stability for the loop. In FIG. 5, step 416 is performed by an optional loop compensator module 530. FIG. 7 illustrates exemplary implementation details of the loop compensation module 530. A variety of other loop compensation modules

suitable for the present invention are available as will be apparent to persons skilled in the relevant art, based on the teachings herein.

In an embodiment, a zero IF FM decoder as described above is implemented in an FRS.

Other advantages of the zero IF FM decoder include tuning reduction, parts reduction, price reduction, size reduction, performance increase, low frequency and power LO, and excellent linearity. Another advantage is that it can down-convert EM signals as high as 3.5 GHz when implemented in CMOS. Higher frequencies can be down-converted using other materials such as GaAs, for example.

Exemplary Environment: Ultra-Low Power Down-Converter

The present invention can be implemented with an aliasing system as disclosed in U.S. Patent Application 09/176,022, titled,"Method and System for Down-Converting Electromagnetic Signals," (hereinafter referred to as the `022 application) incorporated herein by reference in its entirety.

FIG. 1 illustrates an exemplary aliasing system 100 for down-converting electromagnetic (EM) signals, such as an RF input (RF_{in}) signal 102. The aliasing system 100 is an exemplary embodiment of an optimized aliasing system, referred to herein as an ultra low power down-converter.

The exemplary aliasing system 100 includes an aliasing module 110 that aliases an EM signal 112, using an aliasing signal 114, and outputs a down-converted signal 116, as disclosed in U.S. Patent Application 09/176,022, titled,"Method and System for Down-Converting Electromagnetic Signals," (hereinafter referred to as the `022 application) incorporated herein by reference in

its entirety. The aliasing module 110 is also referred to herein as a universal frequency translator (UFT) module.

Aliasing system 100 optionally includes one or more of an input impedance match module 118, a parallel resonant tank module 120, and an output impedance match module 122, as disclosed in the `022 application.

Aliasing system 100 optionally includes a local oscillator (LO) impedance match module 124 for impedance matching a local oscillator input (LO_{in}) signal 126, generated by a local oscillator 128, to the aliasing module 110. The LO impedance match module 124 can be designed to increase the voltage of the LO_{in} signal 126, as illustrated by a higher voltage LO_{in} signal 130. The LO impedance match module 124 permits the aliasing system 100 to efficiently operate with a relatively low voltage LO_{in} signal 126, without the use of power consuming amplifiers that would otherwise be necessary to increase the amplitude of the LO_{in} signal 126.

Unless otherwise noted, the aliasing signal 114 is used interchangeably herein to refer to the LO_{in} signal 126 and/or the higher voltage LO_{in} signal 130.

The aliasing system 100 optionally includes a DC block 132 that substantially blocks DC while passing substantially all non-DC. In the exemplary embodiment, the DC block 132 is a DC blocking capacitor 133. A variety of implementations of the DC block 132 suitable for the present invention are available as will be apparent to persons skilled in the relevant art, based on the teachings herein.

The aliasing system 100 optionally includes a bias module 134 for biasing the aliasing signal 114. A variety of implementations of the biasing module 134 suitable for the present invention are available as will be apparent to persons skilled in the relevant art, based on the teachings herein.

FIG. 2 illustrates an exemplary schematic diagram 202 that can be used to implement the aliasing system 100. The exemplary schematic diagram 202 provides exemplary circuit elements that can be used within the optional input impedance match module 118, the optional parallel resonant tank 120, the optional output impedance match module 122, the optional LO impedance match module, the optional DC block 132, and the optional bias module 134. The invention is not limited to the exemplary embodiment of FIG. 2.

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The exemplary schematic diagram 202 includes a storage module 210 for storing energy transferred from the EM signal 112, as disclosed in the `022 application.

In the schematic diagram 202, the aliasing module 110 of FIG. 1 is illustrated as an application specific integrated circuit (ASIC) 212. In an embodiment, the ASIC is implemented in complementary metal oxide semiconductor (CMOS).

The ASIC 212 is coupled to a first voltage source 218 for supplying power circuits within the ASIC 212. The circuits within the ASIC 212 are described below with reference to FIG. 3. An optional first bypass module 220 is optionally disposed as illustrated to substantially eliminate unwanted frequencies from the first power supply 218 and from the ASIC 212.

The ASIC 212 includes a substrate (not shown) which is optionally coupled to a second voltage source 214. An advantage of coupling the substrate to the second voltage source 214 is described below with reference to FIG. 3. When the substrate is coupled to the second voltage source 214, an optional second bypass module 216 is optionally disposed as illustrated to substantially eliminate unwanted frequencies from the substrate and the second voltage source 214.

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FIG. 3 illustrates an aliasing module 302, which is an exemplary embodiment of the aliasing module 110 and the ASIC 212. The aliasing module

302 includes a sine wave to square wave converter module 310, a pulse shaper module 312 and a switch module 314. The sine wave to square wave converter module 310 converts a sine wave 114 from the local oscillator 128 to a square wave 311. The pulse shaper module 312 receives the square wave 311 and generates energy transfer pulses 313 therefrom. Energy transfer pulses are discussed in greater detail in the `022 application.

In an embodiment, the pulse shaper module 312 is implemented as a mono-stable multi-state vibrator. A variety of implementations of the pulse shaper module 312 suitable for the present invention are available as will be apparent to persons skilled in the relevant art, based on the teachings herein.

Generally, the frequency of the energy transfer pulses 311 is determined by the frequency of the aliasing signal 114 and the width or aperture of the energy transfer pulses is determined by the pulse shaper module 312.

In the illustrated embodiment, where the sine wave to square wave converter module 310 and the pulse shaper module 312 are provided on-chip, the ASIC substrate (not shown) is optionally coupled to the second power supply 214. The second power supply 214 can be varied to affect the performance of the circuits on the ASIC 212, with a result of effectively adjusting the pulse width of the energy transfer pulses 313.

In an alternative embodiment, the sine wave to square wave converter module 310 and/or the pulse shaper module 312 are provided off-chip.

An advantage of the ultra-low power down-converter aliasing system 100 is its low power consumption. For example, in an actual implementation, the aliasing module 302 required an average of approximately 1 mA and consumed approximately 3 to 5 mWatt. This is significantly greater performance than conventional down converter systems.

Other advantages of the ultra-low power down-converter aliasing system 100 include tuning reduction, parts reduction, price reduction, size reduction, performance increase, low frequency and power LO, and excellent linearity. Another advantage of the ultra-low power down-converter aliasing system is that it can down-convert EM signals as high as 3.5 GHz when implemented in CMOS. Higher frequencies can be down-converted using other materials such as gallium arsenide (GaAs), for example.

In an embodiment, an ultra-low power down-converter as described above is implemented in an FRS.

High Efficiency Transmitter

This section describes the high-efficiency transmitter embodiment of a frequency up-converter for use in a family radio service unit. It describes methods and systems related to a transmitter. Structural exemplary embodiments for achieving these methods and systems are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The present invention has significant advantages over conventional transmitters. These advantages include, but are not limited to, a reduction in the number of parts to accomplish the transmitter function, a reduction in the power requirements for the circuit, and a reduction of cost and complexity by permitting the use of circuits designed for lower frequency applications, including, but not limited to, lower frequency oscillators.

An embodiment for transmitting a voice signal is shown in FIG. 8. The voice signal is input to a microphone 802. The output of microphone 802 is an analog voice signal 824 which is connected to an audio amplifier 804. The output of audio amplifier 804 is an amplified signal 826 which is filtered by an audio buffer amplifier 806. Audio buffer amplifier 806 acts as a low pass filter to eliminate unwanted higher frequency signals. The output of audio buffer amplifier 806 is a signal 828 which is accepted by crystal oscillator 808. Crystal oscillator 808 operates as a voltage controlled oscillator and outputs a frequency modulated (FM) signal 830 that is a sinusoidal signal biased substantially around zero volts.

At a node 840, a bias voltage 810 combines with FM signal 830. For the implementation wherein bias voltage 810 is a positive voltage, the bias point of FM signal 830 is raised such that substantially the entire waveform is above zero. In an alternate implementation wherein bias voltage 810 is negative, the bias point of FM signal 830 is lowered such that substantially all of the waveform is below zero. This combination of FM signal 830 and bias voltage 810 results in an FM control signal 832. Substantially all of FM control signal 832 is above zero (or below zero if bias voltage 810 is negative). FM control signal 832 is then input to a universal frequency translator (UFT) module 812.

UFT module 812 is comprised of a pulse shaping circuit and a switch, and is described in detail below in FIG. 9. The output of UFT module 812 is a rectangular waveform 834 that contains a plurality of harmonics. Rectangular waveform 834 is accepted by a filter 816 which filters out the undesired harmonic frequencies and outputs a desired output signal 836. Desired output signal 836 is the frequency modulated signal at the desired output frequency. Desired output signal 836 goes to a driver 818 and then to a power amplifier 820. The output of power amplifier 820 is an amplified output signal 838. Amplified output signal 838 is ready for transmission and is routed to an antenna 822.

The design of UFT module 812 is shown in FIG. 9. FM control signal 832 is accepted by a "square-up" circuit 902 to create a frequency modulated square wave 908 from the sinusoidal waveform of FM control signal 832. FM square wave 908 is then routed to a pulse shaper 904 to create a string of pulses 910. In one embodiment, pulse shaper 904 is a mono-stable multi-vibrator. The string of pulses 910 operates a switch 906 which creates rectangular waveform 834. Typically, pulse shaper 904 is designed such that each pulse in string of pulses 910 has a pulse width "τ" that is substantially equal to $(n/2)\bullet T$, where "T" is the period of desired output signal 836, and "n" is any odd number. As stated previously, switch 906 outputs rectangular waveform 834, which is then routed to filter 816 of FIG. 8. Another input to UFT module 812 is a bias signal 814, which, in this embodiment, is connected to the opposite terminal of switch 906 from rectangular waveform 834.

In one implementation of the invention, switch 906 is a field effect transistor (FET). A specific implementation wherein the FET is a complementary metal oxide semiconductor (CMOS) FET is shown is FIG 11. A CMOS FET has three terminals: a gate 1102, a source 1104, and a drain 1106. String of pulses 910 is shown at gate 1102, bias signal 814 is shown at source 1104, and rectangular waveform 834 is shown at drain 1106. Those skilled in the relevant art(s) will appreciate that the source and drain of a FET are interchangeable, and that bias signal 814 could be at the drain 1106, with rectangular waveform 834 being at the source 1104. Numerous circuit designs are available to eliminate any possible asymmetry, and an example of such a circuit may be found in co-pending U.S. Patent Application 09/176,154, entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, the full disclosure of which is incorporated herein by reference.

FIG. 10 is a detailed schematic drawing of the embodiment described above. Those skilled in the relevant art(s) will appreciated that numerous circuit

designs can be used, and that FIG. 10 is shown for illustrative purposes only, and is not limiting. In addition, there are a variety of commercially available components and assemblies suitable for use in the present invention (e.g., audio amplifiers, audio buffer amplifiers, crystal oscillators, drivers, and power amplifiers) as will be apparent to those skilled in the relevant art(s) based on the teachings contained herein.

Microphone 802 of FIG. 8 is shown as a microphone 1002 in FIG. 10. The output of microphone 1002 is a voice signal which is routed to an audio amplifier 1004 and then to an audio buffer amplifier 1006. A crystal oscillator 1008 is driven by the output of audio buffer amplifier 1006 to create the FM signal 830. A bias voltage 1010 combines with FM signal 830 to create the FM control signal 832. FM control signal 832 is routed to a UFT module 1012 which creates rectangular signal 834. Also connected to UFT 1012 is a bias signal 1012. Rectangular signal 834 is filtered by a filter 1016 to remove the unwanted harmonics and results in desired output signal 836. Desired output signal 836 goes to a driver 1018 and then to a power amplifier 1020. The output of power amplifier 1020 is amplified output signal 838. Amplified output signal 838 is ready for transmission and is routed to an antenna 1022.

In the above implementation, looking back to FIG. 8, the frequency of FM control signal 832 is a sub-harmonic of the frequency of desired output signal 836. It will be understood by those skilled in the relevant art(s) that the selection of the frequencies will have an impact on the amplitude of the desired output signal 836, and will be a determinative factor as to whether or not driver 818 and/or power amplifier 820 will be needed. Similarly, those skilled in the relevant art(s)will understand that the selection of microphone 802 will have an effect on analog voice signal 824, and will be a determinative factor as to whether or not audio amplifier 804 and/or audio buffer amplifier 806 will be needed. Additionally, those skilled in

the relevant art(s) will understand that the specific design of UFT 812 will be a determinative factor as to whether or not bias voltage 810 is needed.

The invention described above is for an embodiment wherein the output of the microphone is described as an analog voice signal. Those skilled in the relevant art(s) will understand that the invention applies equally to a digital signal, either digital data or a voice signal that has been digitized.

Transceiver

The inventions described above can be implemented individually. Alternatively, two or more of the inventions described above can be implemented in combination with one another. For example, one or both of the ultra-low power down-converter and zero IF/FM decoder can be implemented with the high efficiency transmitter described above, as a transceiver. Also, one or both of the ultra-low power down-converter and zero IF FM decoder can be implemented with a transmitter designed in accordance with the disclosure provided in co-pending U.S. Patent Application 09/176,154, titled, "Method and System for Frequency Up-Conversion," filed October 21, 1998, incorporated herein by reference in its entirety.

In an embodiment, a transceiver as described above is implemented as a FRS transceiver.